AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on page 5, line 18 of the specification as follows:

Figure 4 illustrates a schematic of a current sensing switch matrix 100 in accordance with one embodiment of the present invention. As indicated by its name, the detection of a closed switch in the matrix is based on current. Similar to the conventional matrix, only one of the rows is driven low at a time. In the example of Figure 4, 16 switches, S1' through S16', are included and each is coupled to one of 16 resistors, R1' through R16', (e.g., each 240Kohm) respectively. Further coupled to the switches S1'-S16' is a current sensing circuit that includes a transistor (Q1, Q2, Q3, and Q4, e.g., bipolar junction transistors), and at least one resistor (R17, R18, R19, and R20, (e.g., each 240Kohm)~~, and R20,~~ R21, R22, R23, and R24, (e.g., each 4.7Kohm)) for each column, Column_0, Column_1, Column_2, and Column_3, of the switch matrix.

Please amend the paragraph beginning on page 6, line 4 of the specification as follows:

To illustrate operation within the switch matrix of Figure 4, one switch, S6', is show as closed. When Row_1 is driven low by a processor 120 coupled to the current sensing circuit, current flows through R6' and R18, as well as the base to emitter junction of Q2, which is the forward current path indicated by the arrow of Q2, as is well appreciated by those skilled in the art. Note that since only Row_1 is driven low, only the switches on Row_1 (~~S1', S2', S3', or S4'~~ S5', S6', S7', or S8') can switch on the transistors Q1 through Q4, respectively.

Please amend the paragraph beginning on page 6, line 11 of the specification as follows:

With the current flowing through the transistor Q2, the small base current is amplified into a large emitter to collector current. The emitter current is converted into a

voltage by R22. Since the resistor R22 converts the current into a voltage, the current is sensed on Column_1 as logic 1 by the processor 120. The logic 1 on Column_1 indicates to the processor, 120 that the switch S6', at the intersection of Row_1 and Column_1, is closed.

Please amend the paragraph beginning on page 8, line 11 of the specification as follows:

In general, the number of switches that can be supported by a given number of I/O lines for a standard matrix is ~~R + C~~ R × C, where R refers to the number of rows and C refers to the number of columns in the matrix. The number of switches in the matrix of the present invention grows in correspondence with S(S-1), where S refers to the number of scan lines. Notice that the number of switches supported by the conventional matrix grows roughly as 1/4 S^2, whereas with the matrix of the present invention, the number grows as S^2–S. As shown by the following table, for a same number of I/O lines/pins, over three times the number of switches can be supported with the matrix in accordance with the present invention, as compared with the conventional matrix.

Please amend the paragraph beginning on page 11, line 1 of the specification as follows:

By way of example, if S151, S152, and S153 or any combination thereof are closed in addition to S154, then the voltage on ~~SCAN4~~ SCAN5 will be in the range of 1.24V to 5V, depending on the number of switches S151 through S153 that are additionally closed. If switches S115, S125, S135, S141, S142, and S143 are also closed, then the voltage on SCAN5 would be at least 1.09 volts, which is still higher than a silicon diode nominal forward voltage drop of 0.7V, and thus, would still sufficiently indicate a high logic level for a closed switch. Thus, in this example, the threshold used for high and low logic states is about 1.0 to 1.1 volts.